IS 10424 (1982): Guide for design and use of printed boards [LITD 5: Semiconductor and Other Electronic Components and Devices]

BLANK PAGE

# Indian Standard

# GUIDE FOR DESIGN AND USE OF PRINTED BOARDS

( First Reprint MARCH 1996 )

UDC 621.3.049.75 (026 ) : 621.38.038



BUREAU OF INDIAN STANDARDS
MANAK BHAVAN, 9 BAHADUR SHAH ZAFAR MARG
NEW DELHI 110002

 *July* 1983

# Indian Standard

# GUIDE FOR DESIGN AND USE OF PRINTED BOARDS

Printed Circuits Sectional Committee, LTDC 17

| *Chairman* | *Representing* |
|---|---|
| Dr J. Vaid | Peico Electronics & Electricals Ltd, Bombay |
| *Members* | |
| Shri M. A. Godbole ( *Alternate* to Dr J. Vaid ) | |
| Dr P. K. Aditya | Electronics Testing & Development Centre, Chandigarh |
| Shri K. B. Aggarwal | Department of Electronics, New Delhi |
| Shri R. K. Chaturvedi ( *Alternate* ) | |
| Col A. K. Borwanker | Ministry of Defence ( DGI ) |
| Lt Col B. S. Gosain ( *Alternate* ) | |
| Shri T. C. Gosalia | Electronic Component Industries Association, New Delhi |
| Shri P. M. Menon | Hindustan Aeronautics Ltd, Hyderabad |
| Shri V. S. Ramaswamy ( *Alternate* ) | |
| Shri A. K. Misra | Directorate General of Civil Aviation, New Delhi |
| Shri Kanhaiya Lal ( *Alternate* ) | |
| Shri V. Mitter | Hegde & Golay Ltd, Bangalore |
| Shri K. P. Karanth ( *Alternate* ) | |
| Shri K. Nagesh | Bharat Electronics Ltd, Bangalore |
| Shri A. S. Narayana | Bakelite Hylam Ltd, Hyderabad |
| Shri H. S. Vinekar ( *Alternate* ) | |
| Shri A. A. Patankar | Bhabha Atomic Research Centre, Bombay |
| Shri P. B. Deshpande ( *Alternate* ) | |
| Shri S. W. Patwardhan | Formica India Division ( BBTCL ), Pune |
| Shri V. K. Hingne ( *Alternate* ) | |
| Shri K. Radhakrishnan | Rao Insulating Co Pvt Ltd, Bangalore |
| Shri P. Vazir Khan ( *Alternate* ) | |
| Shri K. Raghunathan | Electronics Corporation of India Ltd, Hyderabad |
| Shri R. P. Subramanian | Indian Telephone Industries Ltd, Bangalore |
| Shri M. S. Jayasimha ( *Alternate* ) | |

( *Continued on page* 2 )

( *Continued from page* 1 )

| *Members* | *Representing* |
|---|---|
| Shri A. Sundara Babu | Ministry of Defence ( R & D ) |
| Shri K. C. Chhabra ( *Alternate* ) | |
| Shri Vijay Kumar | Posts & Telegraphs Department, New Delhi |
| Shri Vinay Topa ( *Alternate* ) | |
| Shri R. C. Jain, Head ( Electronics ) | Director General, ISI ( *Ex-officio Member* ) |

*Secretary*

Shri A. S. Rawat
Assistant Director ( Electronics ), ISI

# *Indian Standard*

# GUIDE FOR DESIGN AND USE OF PRINTED BOARDS

## 0. FOREWORD

**0.1** This Indian Standard was adopted by the Indian Standards Institution on 16 September 1982, after the draft finalized by the Printed Circuits Sectional Committee had been approved by the Electronics and Telecommunication Division Council.

**0.2** This standard provides guidance in design and use of printed circuits for use in electronic equipment. The guidance is based on accepted and proven methods used internationally.

**0.3** This standard is intended to apply to normal printed wiring applications but shall not impose limitations on advancement of design.

**0.4** Assistance has been derived in preparation of this standard from IEC Pub 326-3 ( 1980 ): Printed Boards, Part 3: Design and use of printed boards, issued by International Electrotechnical Commission.

---

## 1. SCOPE

**1.1** This standard lays down guiding principles pertaining to the design and application of printed boards, irrespective of their methods of manufacture. However, it does not apply to the fabrication of components such as resistors, capacitors, inductors or transmission lines using these techniques.

## 2. MATERIALS

**2.0 General** — The material for printed wiring boards shall be:

a) Metal-clad base material where the wiring pattern is to be chemically etched and drilled, or

b) Base material where the wiring pattern is formed by plating or by diestamping adhesive coated foil direct on to the base material.

**2.1 Paper Phenolic Sheets** — Phenolic materials are subject to degradation of electrical properties when continuously exposed to high temperature, humidity and sunlight. Paper phenolic sheets suffer serious and

permanent damage when subjected to excessive heating, such as in close proximity to a hot resistor or when a flash over between conductors occurs. In both instances the material is carbonized resulting in a very low insulation resistance. This material is suitable for use up to 100°C. Applied voltage should be limited to 250 V at 25°C reducing to 150 V at 70°C.

**2.2 Paper Epoxide Sheets** — This material is stronger and has better physical properties than the phenolic paper boards and has greater resistance to cracking. The maximum operating temperature is 125°C and there is no pronounced deterioration of electrical properties with ageing. Flame retardant grades are available.

**2.3 Glass Epoxide Sheets** — This material has good mechanical properties and is resistant to shocks. It has good resistance to adverse environmental conditions. The maximum operating temperature is 125°C.

## 3. IMPORTANT CHARACTERISTICS FOR SELECTION OF MATERIAL

**3.1 Thickness** — The lowest overall and copper thickness, commensurate with mechanical properties and current carrying capacity required shall be chosen. The following factors dictate this necessity:

a) The cost of the laminate is directly proportional to thickness.

b) Tool wear is proportional to the thickness of board processed; for instance, a solid carbide bit is normally used to drill only 5 000 holes meant for plating through, in 1·6 mm glass-epoxy material. Beyond this limit the drill bit wears out and produces poor quality holes. Thinner boards allow a corresponding increase in tool life. Thicker boards present problems in shearing, blanking and notching too, since the required edge quality is more difficult to obtain.

c) Plated through holes in thicker boards are less reliable, since they are more sensitive to temperature cycling. This is due to the differential thermal expansion of copper and base laminate ( *see* Table 1 ) and due to the reduced ' throwing ' of copper plated deposit in the hole centre.

d) The etching time is directly proportional to the thickness of copper plating. Thickly clad sheet requires more chemicals also.

e) Thicker copper causes greater ' undercut ' and poorer ' definition '.

**3.2 Dimensional Stability** — Due to the composite nature of copper clad laminates the material suffers from internal stresses impressed during the laminate manufacture. This causes the material to change in dimension during various manufacturing processes.

During etching the material shrinks/expands in a rather unpredictable manner, to the extent of 0·1 to 0·5 percent. ( That is, two holes 100 mm apart, may shift 0·5 mm after etching ).

Thermal expansion, for instance due to wave soldering, also causes instability, since the material does not completely return to its original dimension after cooling. Further, the expansion is not uniform in all directions, as shown in Table 1.

**TABLE 1 THERMAL EXPANSION, $10^{-5} \times$ mm/mm °C**

( *Clauses* 3.1 *and* 3.2 )

| Axix (1) | Paper Phenolic (2) | Glass Epoxy (3) | Copper (4) |
|---|---|---|---|
| Along the grain ( lengthwise ) | 2 | 1·1 | 1·7 |
| Across the grain ( crosswise ) | 4 | 1·5 | 1·7 |
| Along thickness ( 'Z' axis ) | 20 | 6 | 1·7 |

The expansion of the material during wave soldering is not the same for copper and the base material. This tends to lift the foil off the base ( also causing great stress on the copper in plated-through holes ). Hence, registration of copper pattern to holes is more critical for long boards. Long boards are also more likely to suffer copper foil lift off during wave soldering. These factors tend to reduce the production yield in the case of a long board.

To minimise these problems:

a) The required board area must be achieved without resorting to long boards.

b) The board/blank should be laid out on the laminate in such a way that the longer dimension falls along the grains. This may be specified by a note on the detail drawing.

c) For critical applications glass epoxy base material should be specified.

**3.2.1** The reliability of plated-through holes depends to a great degree on the dimensional stability and the low thermal expansion ( along the thickness ) of the base material. The cost difference between glass epoxy and paper phenolic materials does not justify the potential loss in reliability entailed by the high 'Z axis' expansion of paper phenolics. These two factors strongly suggest that only glass epoxy based material should be used for double sided boards.

**3.3 Dielectric Constant and Dissipation Factor** — Paper phenolic laminates have a higher dielectric constant and dissipation factor. The dielectric losses hence are higher than those of glass epoxy laminates. Paper phenolic also absorbs more water than glass epoxy. Dielectric constant of water is very high and the dissipation increases steeply with frequency. This is reflected in the printed circuit board laminate behaviour also. Hence, paper phenolics are not recommended for use in high humidity environments nor at high frequencies.

## 4. DIMENSIONS

**4.1 Outline Dimensions of Printed Boards** — In principle, a printed board may have any shape, but a simple shape may often facilitate the production.

Unless the quantity to be manufactured justifies special production means, the size of a printed board will normally be limited by the available production facilities and also by stability requirements.

The tolerances on outline dimensions achievable for printed boards are the same as is usually obtainable for materials similar to those used for base materials. Care should be taken to avoid unnecessarily tight tolerances which may cause difficulties and may increase costs.

**4.2 Board Thickness**

**4.2.1** *Single and Double Sided Printed Boards* — The values of nominal board thicknesses are:

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 0.2 | 0.5 | 0.7 | 0.8 | 1.0 | 1.2 | 1.5 | 1.6 | 2.0 | 2.4 | 3.2 | 6.4 |

NOTE — The table sums up all values given in all specifications of IS : 5921 and IS : 7405 series.

The total board thickness will deviate from the board thickness ( and the relevant tolerance ) when additional platings or other coatings are applied. A tolerance on the total board thickness is important in the zone of edge board contacts or other printed contacts.

**4.3 Dimensions of Holes**

**4.3.1** *Plain Holes* — The following nominal hole diameters and deviations from nominal are recommended:

| Nominal Hole Diameter (mm) | Deviation (mm) |
|---|---|
| 0·4<br>0·5<br>0·6<br>0·8<br>0·9 | ±0·05 |
| 1·0<br>1·3<br>1·6<br>2·0 | ±0·1 |

**4.3.2** *Plated-through holes*

**4.3.2.1** The ratio hole diameter/board thickness should preferably be not less than 1 : 3. Smaller ratios may cause production difficulties and increase the cost.

**4.3.2.2** Where a plated-through hole is intended to be used for a through connection or an interlayer connection only, the tolerance on hole diameter, particularly the minimum hole diameter, is usually not important.

Where a plated-through hole is intended to be used as a component hole, the minimum diameter of a plated-through hole shall be not less than the minimum diameter of the plain hole ( with the same nominal diameter ) as calculated from the values recommended in **4.3.1**, in order to fit the terminations of the component or sub-assembly.

Hence the following nominal and minimum diameters are recommended for component holes:

| Nominal Hole Diameter (mm) | Minimum Hole Diameter (mm) |
|---|---|
| 0·4 | 0·35 |
| 0·5 | 0·45 |
| 0·6 | 0·55 |
| 0·8 | 0·75 |
| 0·9 | 0·85 |
| 1·0 | 0·9 |
| 1·3 | 1·2 |
| 1·6 | 1·5 |
| 2·0 | 1·9 |

The maximum diameter of a plated-through hole depends on the plating thickness and the tolerances of plating thickness and of hole diameter.

Minimum plating thickness will usually be specified and deviations in plating thickness of 0 to +100% will generally apply.

It is recommended that the average thickness of the copper plating in a hole be not less than 25 $\mu$m with a minimum thickness of about 15 to 18 $\mu$m. If necessary this should be verified by a suitable test, for example microsectioning.

**4.4 Dimensions of Slots and Notches** — In principle, slots, notches etc, of any reasonable size and shape are feasible as with other laminated materials similar to those used for base materials.

For plain slots, notches, etc, deviations of $\pm 0 \cdot 1$ mm for length and width are suggested.

**4.5 Dimensions of Conductors**

**4.5.1** *Conductor Width* — The conductor width should normally be chosen as large as possible for the particular design or layout of the conductive pattern but at least large enough for the current load to be expected.

The accuracy of the conductor width obtainable on the board depends on several factors, for example the accuracy of the production master, the production process ( method of printing, application of additive or subtractive process, method of plating, quality of etching ) and the uniformity of the conductor thickness.

To specify conductor width, either tolerances, i.e. design width and permissible deviation, or minimum conditions may be specified.

**4.5.1.1** *Tolerances* — If tolerances are to be used, it must be specified and agreed between purchaser and vendor, which width shall be the design width to which the permissible deviations are related.

NOTE — The width in the original production master is often used as design width, but in that case the original production master must be approved by the purchaser.

Independent of the conductor width, the following permissible deviations are recommended:

| | Extra Fine | Fine | Normal | Coarse |
|---|---|---|---|---|
| Normally no plating process included (mm) | $+0 \cdot 03$<br>$-0 \cdot 05$ | $+0 \cdot 05$<br>$-0 \cdot 1$ | $+0 \cdot 1$<br>$-0 \cdot 13$ | $+0 \cdot 15$<br>$-0 \cdot 25$ |
| Normally plated on metal is used (mm) | $+0 \cdot 03$<br>$-0 \cdot 05$ | $+0 \cdot 08$<br>$-0 \cdot 05$ | $+0 \cdot 15$<br>$-0 \cdot 1$ | $+0 \cdot 3$<br>$-0 \cdot 2$ |

These deviations are based on 35 $\mu$m basic copper thickness and a normal plating thickness. Any other thickness of metal may require different tolerances.

A systematic deviation of the conductor width caused by a given process may also be compensated by a corresponding change of the conductor width in the artwork.

Imperfections, such as nicks, pinholes, holes or edge defects are not included in these deviations, but may occur. These imperfections are normally acceptable provided the conductor width is not reduced by more than an amount, usually 20 percent or 35 percent, specified in the relevant specification. If the current-carrying capacity is utilized to a high degree, the imperfection must be duly taken into account.

**4.5.1.2** *Minimum conditions* — In certain cases it will be sufficient and even easier and more compatible with the actual requirements to specify minimum conditions only.

If minimum conditions are to be used, the minimum conductor width permitted must be specified. It must also be stated whether the minimum conductor width specified is the absolutely irreducible miniumum value or whether imperfections, such as nicks, pinholes, holes or edge defects are permitted to reduce the specified minimum conductor width additionally.

**4.5.2** *Spacing Between Conductors*

**4.5.2.1** The spacing between adjacent conductors shall be as wide as necessary to suit the electrical safety requirements, and as wide as possible to facilitate handling and production.

**4.5.2.2** The minimum spacing shall be chosen at least so as to be suitable for the voltage applied. This voltage may embrace the normal operating voltage and additional ripple, over-voltage, surges or peaks that may occur repeatedly or sporadically during normal operation or in the event of malfunction. The applicable or specified safety requirements must be accordingly taken into account. Some information on the relation between conductor spacing and applicable voltage is given in **7.4**.

The spacing may be reduced if the relevant specification permits particles between conductors. Any reduction of the spacing due to metallic particles between conductors must duly be taken into account when considering the voltage problem.

A spacing over a certain value, for example 0·5 mm may facilitate handling and production. For instance, the influence of deviations and imperfections is smaller, there is less danger of bridging during the soldering operation.

NOTE — The value is only meant to show the tendency, not a limit. A generally applicable limiting value cannot be given, since it depends too much on the process used and the available production facilities.

**4.5.2.3** *Tolerances* — Since the tolerances on conductor spacings depends not only on the positional deviations of the conductor but also on the deviation of the conductor width, tolerances for the spacing between conductors can only be specified if tolerances are specified for the conductor width also.

The relation between nominal spacing and minimum spacing is given by the following formula:

$$d_{min} = d_{nom} - \triangle d$$

where

$d_{min}$ = minimum spacing between conductors,

$d_{nom}$ = nominal spacing between conductors as in the production master, and

$\triangle d$ = the influence of the deviation of the conductor width.

a) $\triangle d$ is twice the value of the upper ( plus ) deviation allowed for the conductor width, if the deviation is likely to enlarge the conductor only on one side.

b) $\triangle d$ is equal to the value of the upper ( plus ) deviation allowed for the conductor width, if the deviation is likely to enlarge the conductor evenly on both sides.

**4.5.2.4** *Minimum conditions* — In certain cases it will be sufficient and even easier and more compatible with the actual requirements to specify minimum conditions only. If minimum conditions are specified for the conductor width, only minimum conditions can be specified for the spacing.

If minimum conditions are to be used, the minimum conductor spacing permitted shall be specified. It shall also be stated whether the minimum conductor spacing specified is the absolutely irreducible minimum value or whether imperfections such as particles between the conductors are permitted to reduce the specified minimum conductor spacing additionally.

**4.5.3** *Position of Patterns and Holes*

**4.5.3.1** *Datum reference* — To locate patterns ( including hole pattern ) for manufacturing or inspection purposes, the use of a datum reference is recommended. Where a printed board contains more than one pattern, the same datum reference should be used for all patterns.

The datum reference should preferably be specified by the designer. One method often applied is the use of two perpendicular lines.

**4.5.3.2** *Positional tolerance of hole centres* — The positional tolerance specifies the diameter of a cylinder whose axis is at the specified position of the hole and in which the centre of the actual hole must be contained.

The positional tolerance obtainable in practice depends mainly on the manufacturing method and facilities. The following tolerances are recommended:

| | Distance between specified position of the hole and datum reference | |
|---|---|---|
| | Up to and including 150 mm (mm) | Over 150 mm (mm) |
| Extra fine | 0·05 | 0·1 |
| Fine | 0·1 | 0·2 |
| Normal | 0·2 | 0·4 |
| Coarse | 0·4 | 0·8 |

When the distance of the specified position of the hole from the datum reference is 150 mm or less in one direction and over 150 mm in the other direction, the larger value for the positional tolerance applies.

**4.5.3.3** *Distance between holes* — The deviation on the distance between any two holes will be the positional tolerance as given in **4.5.3.2**.

NOTE — Deviation = ± ( radius positional tolerance hole 1 + radius positional tolerance hole 2 );

± ½ ( positional tolerance hole 1 + positional tolerance hole 2 ).

**4.5.3.4** *Misalignment of hole and land* — For printed boards using holes and lands, misalignment of hole and land will normally occur since the conductive pattern and the hole pattern are made in different production steps. The application of the same datum reference for both patterns as recommended in **4.5.3.1** will reduce the misalignment but cannot eliminate it.

If not specified by the relevant specification or if the limiting value specified there is not acceptable for a particular design, the designer should specify this important feature taking into account the requirements of his particular design.

**4.5.3.5** *Pattern position relative to datum reference* ( *registration* ) — This need normally not be specified for single and double sided printed boards using holes, and lands, as the important feature in that case is the relationship between pattern and holes, which controls the minimum radial land width.

For other types of printed boards, however, particularly for printed boards using landless holes and for the thin printed boards intended to be used as layers of a multilayer printed board, the pattern position relative

to the datum reference may be important. This may even be the only possible way to test the thin printed boards before the multilayer printed board is made.

Where the registration of pattern position relative to a datum reference is specified, the following deviations are recommended:

| | |
|---|---|
| Fine | $\pm 0 \cdot 05$ mm |
| Normal | $\pm 0 \cdot 1$ mm |
| Coarse | $\pm 0 \cdot 25$ mm |

**4.5.3.6** *Side-to-side pattern registration* — This need not be specified separately. The value may be obtained from the deviations specified for the pattern position relative to the datum reference. Side-to-side pattern registration deviation will be twice the deviation specified for the pattern position relative to the datum reference.

## 5. SURFACE FINISHES

### 5.1 Metallic Finishes

**5.1.1** A suitable finish for the conductive pattern should be chosen, depending on the application of the printed board. The type of surface finish may influence the production process, the production costs and the properties of the printed board; for example shelf-life, solderability, contact properties.

Examples of widely used surface finishes are given below. These contain thickness values because of variations in applications.

a) Copper: without additional plating. Often used for simple single-sided printed boards (print and etch technique) and for printed boards with plated-through holes (e.g. tenting, additive or semi-additive processes) without special finish requirements. Usually a temporary protective coating is applied.

b) Tin-lead or tin: used to preserve solderability.

NOTE — Long-term solderability of tin-lead may be improved by reflowing, but after reflowing there is usually only a very thin layer of tin-lead left at the transition between land and wall of the hole. The solderability at this transition may be inferior to that at other areas.

c) Gold
d) Gold on nickel
e) Rhodium on nickel
f) Rhodium on nickel and gold
g) Tin-nickel

} Usually used for printed contacts.

Different finishes may be used on different parts of the same board, but production costs may be affected by this.

**5.1.2** Where printed contacts are used, care should be taken to apply a type of plating compatible with the counter-part. No general rule can be given since the appropriate plating depends on several factors most of which are interrelated, for example:

a) Type of plating of the counter-part;
b) Design of counter-part ( shape, contact pressure, etc );
c) Endurance, number of operations expected;
d) Electrical requirements ( e.g. contact resistance ) and
e) Mechanical requirements ( e.g. insertion/withdrawal forces ).

The metal surface of the printed contact shall be smooth and free from defects likely to cause reduction in either electrical or mechanical properties.

**5.2 Non-metallic Finishes**

**5.2.1** The surface of a printed board may also have non-metallic finishes. Such finishes and their purpose are for example:

a) Coating to preserve the solderability of the conductive pattern.

b) Solder-resists to prevent wetting of defined areas and bridging between parts of the conductive pattern.

   Normally the solder resist is not removed after the soldering operation and serves as a permanent protective coating;

c) Coating to improve and/or maintain the electrical properties of the board. This type of coating may be applied before or after the soldering operation.

## 6. ASSEMBLY

**6.1** The terminations of the components/sub-assemblies will be connected to the conductive pattern using:

a) plain holes with lands;
b) plated-through holes with lands;
c) landless plated-through holes;
d) lands without holes ( surface mounting );
e) other techniques, e.g. punched-through pins/eyelets.

The connections shall preferably be located on a grid as recommended in Appendix A. The grid spacing shall be chosen so as to suit the particular application.

The connection should be located on the crosspoints of the grid lines. The position of the conductors, however, is independent of the grid; the conductors may not necessarily follow the grid lines.

## 7. ELECTRICAL CHARACTERISTICS

### 7.1 Resistance

**7.1.1** *Resistance of Conductors* — If important, the resistance of conductors shall be determined. For copper as conductive material having a resistivity of $Q = 1 \cdot 8 \times 10^{-6}\ \Omega$ cm and conductors of constant width, Fig. 1 gives the correlation between conductor width, thickness and temperature and the resistance per 10 mm conductor length.

Thin platings, particularly of materials such as nickel, gold or tin, can be disregarded in many cases, as they are normally of little influence.

Thick platings of materials having relatively low resistivity, for example, copper plating usually present on printed boards with plated-through holes, must duly be taken into account. Where a rough estimation is sufficient, the resistance of a conductor with additional thick copper plating may be evaluated by adding the plating thickness to the thickness of the copper foil and estimating the resistance from Fig. 1.

For materials of the conductive foil other than copper, or other shapes of the conductor, the resistance of the conductor must be calculated, if required.

**7.1.2** *Resistance of Interconnections* — The resistance of an interconnection between two plated-through holes on a multilayer printed board consists normally of:

— the part $R_1$ of the plating in a plated-through hole;
— the part $R_2$ of the connection between that plating and a conductor on an internal layer;
— the part $R_3$ of that conductor;
— the part $R_4$ of the connection between that conductor and the plating in a second plated-through hole;
— the part $R_5$ of that plating.

The parts contributing to the total value are normally not accessible.

If important, the resistance of the interconnections shall be determined.

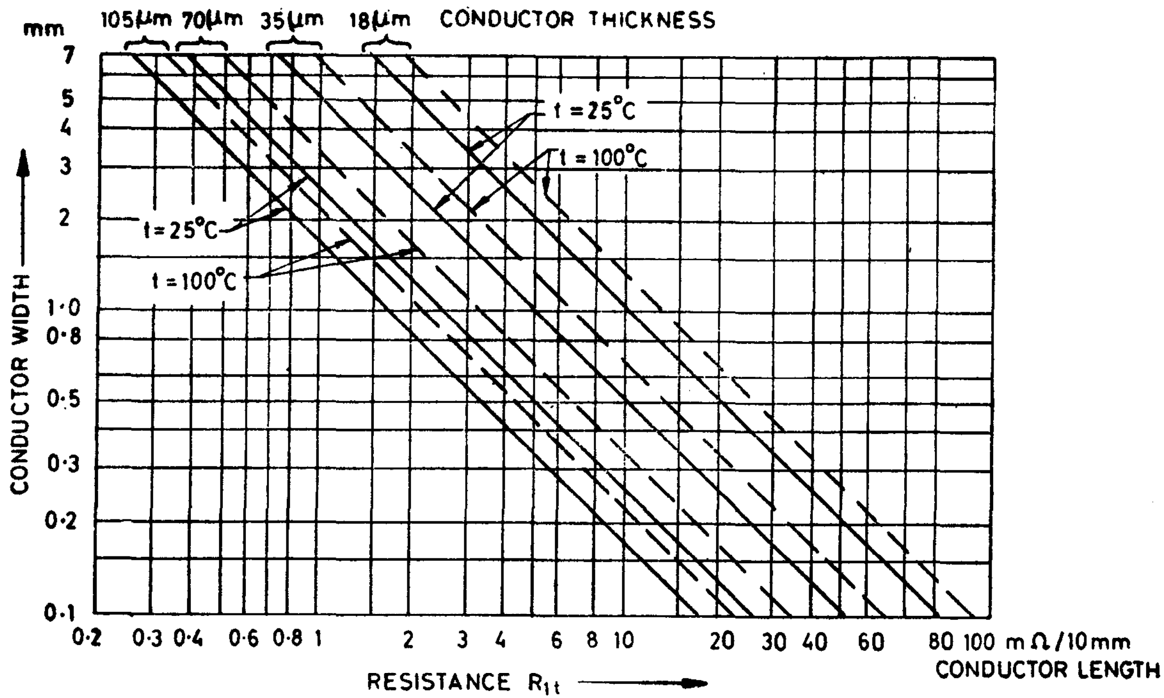



Fig. 1 Conductor Width and Resistances

While the conductor part of the interconnection resistance may be determined as described in **7.1.1**, the total interconnection resistance can be determined only by electrical measurement.

It may be advantageous to include the test and requirements in the relevant specification, even if the value of the interconnection resistance is not important for the electrical circuit, since it gives an indication of the quality of the processes used in the production.

**7.1.3** *Resistance of Plated-Through Holes* — The value of the resistance of a plated-through hole is normally not important for the electrical circuit. It may be advantageous, however, to include the test and requirements for the change in resistance due to thermal stress testing in the relevant specification, since they give an indication of the quality of the plating and hence of the processes used in the production.

When a printed board is heated, for example by immersion into a hot oil bath, the resistance of the plating in a plated-through hole increases:

a) due to the normal dependency of the resistance on the temperature; this process is normally reversible;

b) due to defective plating; in this case, the change in resistance may be reversible but bigger than normal, but it may also be non-reversible to some extent leaving a permanent change in resistance after each thermal cycle.

Figure 2 has been prepared as an aid in estimating the resistance of the plating in a hole. It applies to board thickness of 1·6 mm and copper plating.

**7.2 Current-Carrying Capacity**

**7.2.1** *Continuous Current, Single External Layers*

**7.2.1.1** Where the current-carrying capacity is important and/or an estimation is not sufficient, the current-carrying capacity must be determined by measuring the temperature rise of the conductors under load. Care must be taken to cover the extreme operational ( electrical and ambient ) conditions and to use the fully assembled and fully loaded printed board.

In many cases, however, estimation may be sufficient. Figure 3 ( a, b, c and d ) has been prepared as an aid in estimating temperature rises against current for various conductor widths and the most common conductor thicknesses.

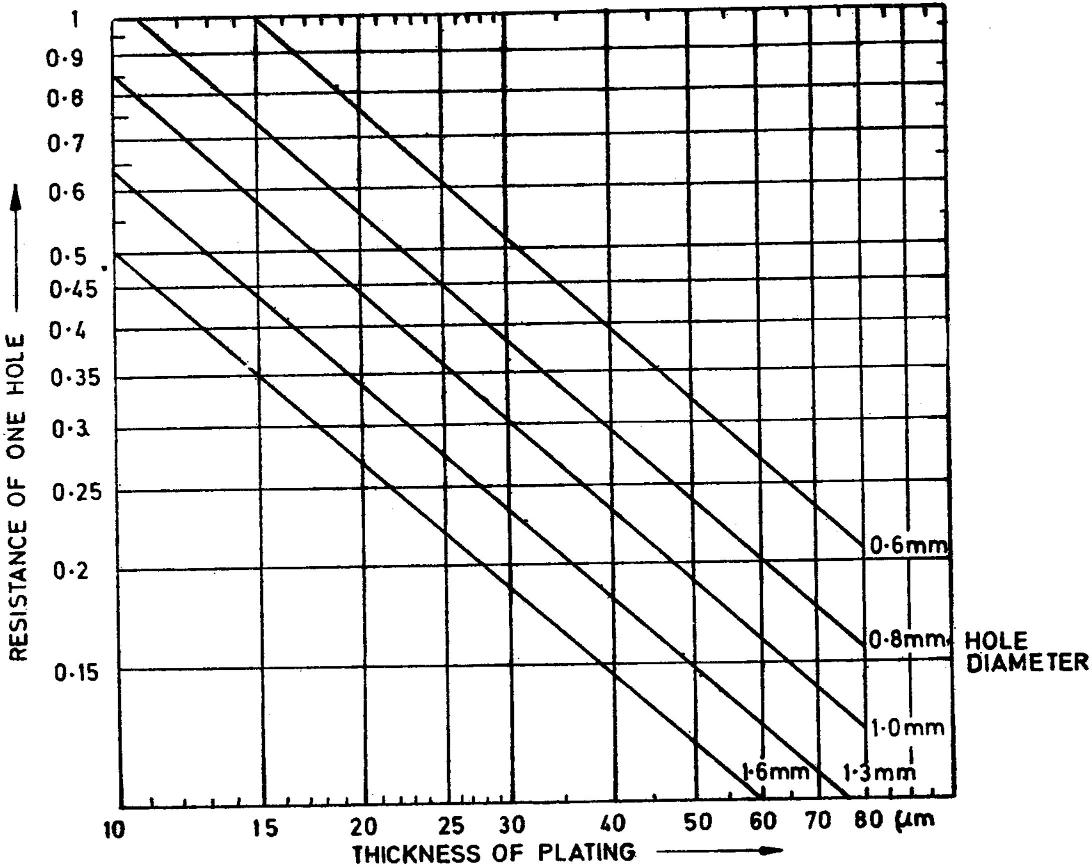



Fig. 2 Resistance of Plating in Hole

**7.2.1.2** The diagrams apply to single-sided printed boards of 1·6 mm to 3·2 mm nominal thickness using copper as conductive material. Additional platings, such as nickel, gold or tin are disregarded. It is further assumed that normal design conditions prevail where the conductor spacings are equal or larger than the conductor widths.

The curves as presented include a 10% derating to allow for normal variations in processing, copper thickness, and conductor width variations. The curve for 105 μm includes an additional 15% derating.

Additional derating of 15% is suggested

a) for board thicknesses 0·5 mm to 1·5 mm;
b) if coating is applied; and
c) if conductor spacings are smaller than conductor widths.

For groups of similar parallel conductors, if closely spaced and loaded with nearly equal currents the temperature rise may be found by adding the conductor widths and the currents.

If the conductors are plated with copper, the plating thickness is added to the thickness of the copper foil and the current-carrying capacity may be estimated by using the curve for the nearest thickness.

**7.2.2** *Surge Current* — The degree of heating of a conductor on a printed board due to current depends on the resistance of the conductor, value and duration of the current and the cooling conditions which are also influenced by the type of the base material.

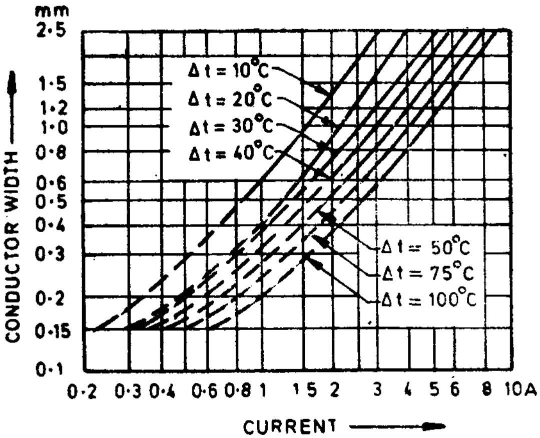
Overload of a conductor does not only strain the adhesion between conductor and base material directly by the influence of heat and temperature, but the high short-circuit currents and the heat expansion will also exert considerable mechanical forces.

The following Fig. 4 ( a and b ) are given for information. They are intended to be used as an aid in estimating permissible short-circuit currents and associated durations for three conductor widths and two thicknesses. No deterioration has been observed in practice when using them as limiting curves. They may, therefore, be utilized when determining fuses or other current limiting means.

### 7.3 Insulation Resistance

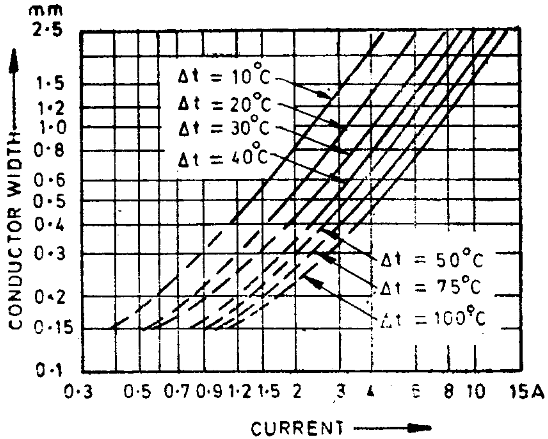
**7.3.1** *Insulation Resistance on Surface Layers*

**7.3.1.1** The insulation resistance depends on the configuration of the relevant part of the conductive pattern, the base material and the processes used as well as on ambient conditions such as temperature, humidity and contamination of the surface.



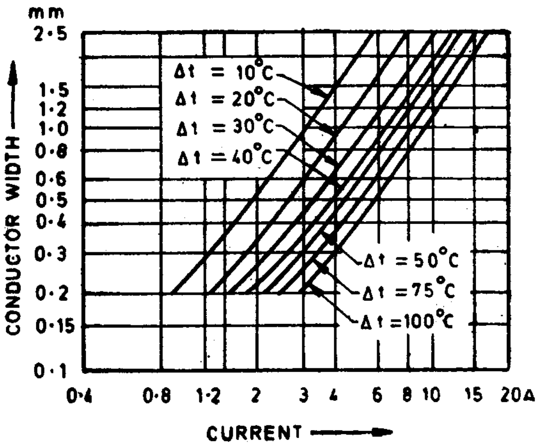

Conductor thickness 18$\mu$m

3 (a)



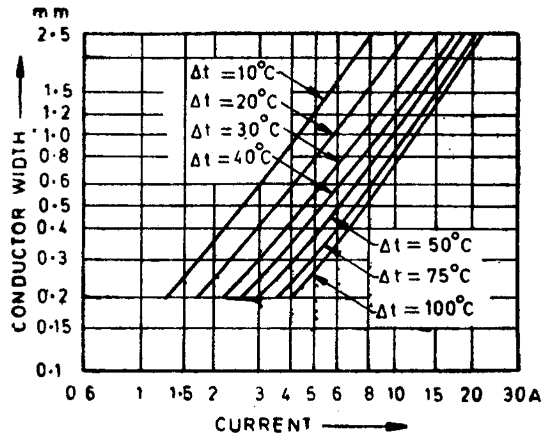

Conductor thickness 36$\mu$m

3 (b)




Conductor thickness 10 $\mu$m

3 (c)




Conductor thickness 106 $\mu$m

3 (d)

FIG. 3 TEMPERATURE RISE WITH CURRENT

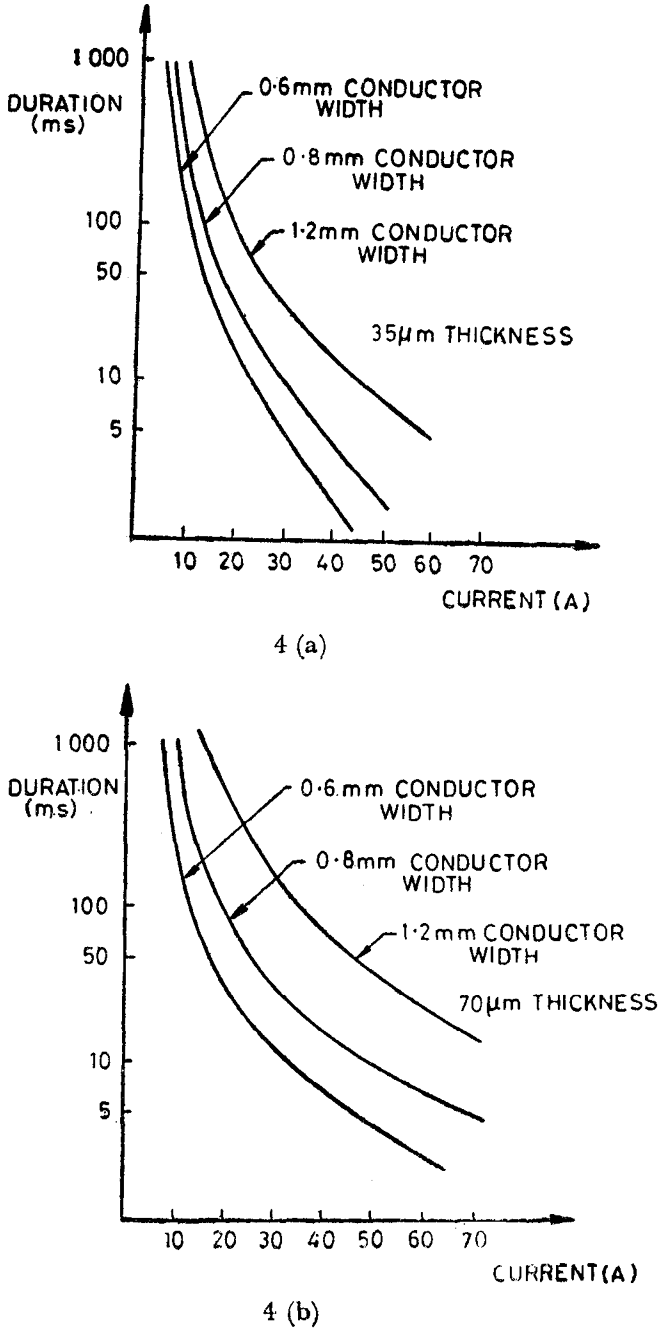



FIG. 4 PERMISSIBLE SHORT-CIRCUIT CURRENT DURATIONS

Provided that appropriate processes are used and that the surface of the printed board is not contaminated, the insulation resistance between a pair of conductors uniformly spaced over a suitable length may be calculated from the following formula:

$$R_{is} = 160 \cdot R_{mat} \cdot \left(\frac{w}{l}\right)$$

where

$R_{is}$ = the minimum insulation resistance that can be expected between the conductors chosen,

$R_{mat}$ = the minimum insulation resistance specified in IS : 5921 for the material at specified temperature,

$w$ = the spacing between the conductors, and

$l$ = the length of the parallel conductors.

Where the spacing $w$ is not uniform in the design, a mean average value for $w/l$ may be calculated from the following formula:

$$\frac{1}{w/l} = \frac{1}{w_1/l_1} + \frac{1}{w_2/l_2} + \ldots\ldots + \frac{1}{w_n/l_n}$$

The subscripts indicate the section length $l_1 \ldots\ldots l_n$ with the various nominal spacings $w_1 \ldots\ldots w_n$.

**7.3.1.2** Attention should be paid to the fact that the insulation resistance values calculated as described here are material values. Owing to many influences, such as plating and soldering processes, contamination, dust, operating conditions, etc, the printed board used in a printed board assembly will show lower insulation resistances. Values of 1 to 3 powers of ten lower than those calculated in accordance with **7.3.1** have been found in practice even under standard atmospheric conditions. The values may even be much lower under severe operating conditions.

Where a multilayer printed board or a double-sided printed board using through connections is considered, care must be taken to avoid, or to take into account, the influence of other parts of the printed board that might be in parallel.

## 7.4 Voltage proof

**7.4.1** *Voltage Proof of Surface Layers* — The voltage permissible between conductors depends on a great variety of factors such as spacing, type of base material, coating, environmental conditions and last but not least the applicable or specified safety rules. No generally applicable requirements can therefore be given.

Coating of a printed board may influence the voltage permissible between conductors. A suitable coating assists in preserving the quality of the printed board when it is subject to adverse conditions, such as dust and damp.

No general rule can be given since quantity and direction of the influence depend on several factors, for example ambient conditions, thickness and material of coating.

If no particular safety rules are specified and no special experience is available, Fig. 5 is given for information:

**7.4.2** *Voltage Proof Between Layers* — The permissible voltage between adjacent layers depends on the thickness and the dielectric strength of the insulating layer and may directly be calculated from the values specified for the insulating materials.

## 8. MECHANICAL CHARACTERISTICS

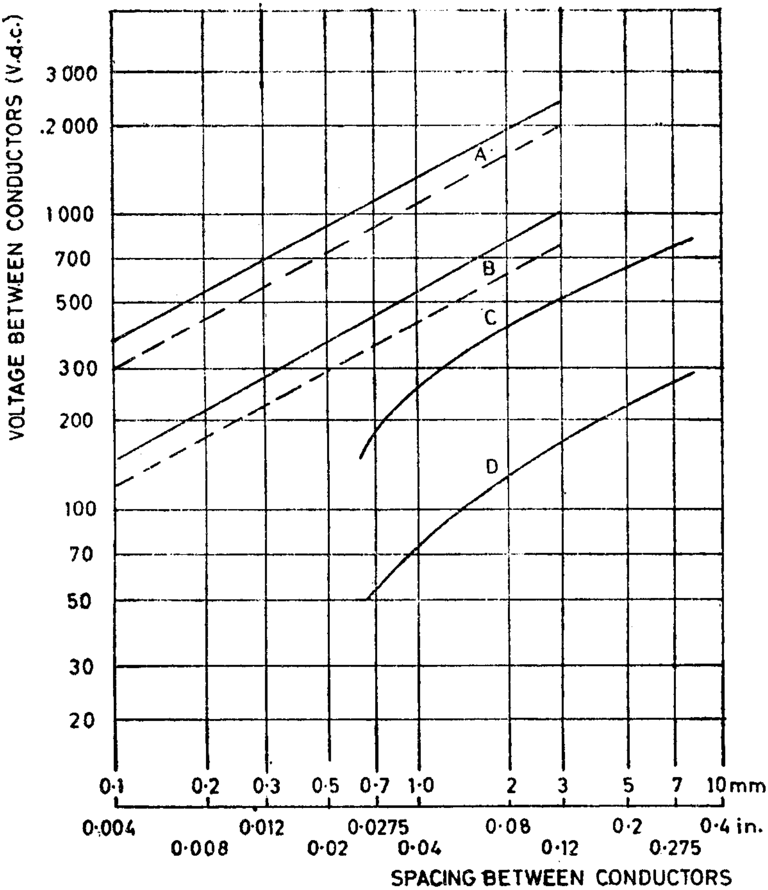
### 8.1 Adhesion of the Conductive Pattern

**8.1.1** *Peel Strength of Conductors* — The adhesion of a conductor to the base material depends on a great variety of factors, such as conductor width, temperature, metal-clad base material, processes, coatings, previous temperature stresses, due for example to soldering operations.

The adhesion of a conductor is usually expressed as peel strength, i.e. as the force per unit width required to peel off the conductor from the base material. The following values of peel strength can be expected for conductors over 0·8 mm width and at normal ambient temperatures:

| Base Material | Minimum Peel Strength (N/mm) |
|---|---|
| Paper phenolic | 0·8 |
| Paper epoxide | 1·1 |
| Glass fabric epoxide | 1·1 |
| Glass fabric PTFE | Under consideration |

For conductors below 0.8 mm width the values may be lower as the influence of small imperfections in the adhesive layer will relatively increase.




| | | | |
|---|---|---|---|
| *Curve A:* | Partial discharge voltage | uncoated, epoxide woven-glass fabric, chemically inactive dust | |
| *Curve B:* | Operating voltage where a derating factor of 2·5 is appropriate | ——— = in rooms up to 1 000 m altitude<br>– – – – = outside buildings but closed, up to 1 000 m altitude | |
| *Curve C:* | Operating voltage where a derating factor of approximately 5 is appropriate | uncoated, up to and including 3 000 m | These curves have been used for many years with good results in the range of larger conductor spacings |
| *Curve D:* | Operating voltage where a derating factor of approximately 11 is appropriate | uncoated, up to and including 15 000 m | |

NOTE — For spacings over 8 mm, the relations between voltage and spacing have to be determined for each case.

**FIG. 5 VOLTAGE AGAINST SPACING BETWEEN CONDUCTORS**

**8.1.2** *Adhesion of Lands at Plain Holes* — The adhesion of a land to a base material depends on a great variety of factors, such as land area, temperature, metal-clad base material, processes, previous temperature stresses, due for example to soldering operations, etc.

The adhesion of a land is usually expressed as pull-off strength, i.e. as force normal to the surface of the printed board required to separate the land from the base material.

**8.1.3** *Pull-out Strength, Plated-Through Holes* — An important factor is the adhesion of the plating to the wall of the hole. Where plated-through holes with lands on one or both sides of a printed board are used, the pull-out strength is a combination of:

— the pull off strength of the upper land;
— the pull out strength of the plating at the wall of the hole; and
— the retention strength of the land at the opposite side of the board.

Where information on the adhesion of the plating to the wall of a hole is sought, only landless plated-through holes should be considered.

The pull-out strength of a landless plated-through hole depends on the diameter and the roughness of the wall of the hole and the thickness of the printed board.

The pull-out strength is usually expressed as the force normal to the surface of the printed board required to separate the plating of the hole from the base material.

The force is exerted on a wire soldered into the hole under test.

The pull-out strength normally achieved in practice is in the order of magnitude of the tensile strength of the wires normally used for component terminations.

**8.2 Flatness**

**8.2.1** Flatness of the printed board is important for the printed board assembly, i.e. the printed board with the components mounted and the soldering operation completed. Undue deviation from flatness may cause difficulties, for example,

— reduction of clearance distances where the printed board is mounted parallel to another board or to shielding parts;
— difficult or even impossible insertion into narrow guides;
— mechanical load of components and solder joints ( with the danger of failure after some time ).

**8.2.2** If necessary, particularly with larger printed boards, provision should be made to prevent undue deviation from flatness, for example by using appropriate reinforcement or stiffening means. Since the soldering operation influences the flatness, it is recommended that the stiffening means be mounted prior to mounting and soldering the components.

**8.2.3** The flatness of a printed board depends on several factors, for example the material used, the production processes used, the hole pattern, the conductive pattern ( even distribution of metal will normally give better flatness ), size and type of the board. Hence there is no direct correlation between the deviation from flatness of

— the metal-clad base material;

— the printed board; and

— the printed board assembly ( components mounted and soldered ).

## 9. MISCELLANEOUS

### 9.1 Soldering

**9.1.1** Usually a mass soldering method will be applied. In this case, the entire metal surface of the solder-side of the printed board will be covered with solder except the portions protected by a solder resist.

To avoid heat sinks and to reduce mechanical stresses, large conductive areas should be broken up by cross-hatching.

Certain arrangements of conductors in the conductive pattern give better results when mass soldered ( for example less bridging ) than others.

**9.1.2** Where a printed board with plated-through holes contains more than one conductive layor, the solder flow in the plated-through hole will be impaired by the amount of metal acting as heat sink on the other layers ( inner layer and/or component side ).

**9.1.3** The solderability of a printed board depends also on the type of surface finish and deterioration due to adverse storage conditions. For bare copper surfaces, usually a temporarily protective coating is applied. Often the entire surface of the conductive pattern is covered with tin-lead ( solder ) or tin to preserve solderability, and the long-term solderability of tin-lead may be improved by reflowing.

**9.1.4** When printed boards are to be packaged, care should be taken to avoid any contamination likely to impair solderability.

When printed boards are stored prior to the soldering operation, the storage conditions, i.e. temperature, humidity, air pollution and storage time will influence the solderability. When carrying out solderability tests, the influence of the storage may be stimulated by an accelerated ageing.

Special attention should be given to protection of edge board contacts during all stages of manufacture, assembly and transit.

**9.1.5** The soldering operation may be carried out using either non-activated or activated flux. It should be noted, however, that in many fields of application activated flux is not permitted and the use of non-activated flux is specified by the user of the equipment containing the printed board. In this case, non-activated flux should also be used when testing the solderability.

If the conductive pattern is overplated with a material that melts, legends and/or solder masks applied on the overplating may cause problems during mass soldering.

**9.2 Delamination** — After a thermal shock, due for example to the soldering operation, printed boards may show delamination.

Delamination may occur due to incorrect processing or inappropriate materials. To determine that correct processing and suitable materials have been used by proving the ability of the printed board to withstand a specified thermal shock without evidence of delamination.

Delamination may also occur due to absorbed humidity. It may be necessary, therefore, that printed boards be dried prior to the soldering operation.

## 10. PACKAGING OF PRINTED BOARDS

**10.1 General** — In order to preserve the original good solderability of printed boards they must be protected by suitable packaging.

The packaging will need to give protection against humidity, contamination due to handling and atmospheric contamination such as ozone, sulphur dioxide, hydrogen sulphide and nitrogen dioxide.

The type of packaging and material used will depend upon the period of storage and — where known — the severity of the storage environment. As a general rule, the better the protection the higher the packaging cost.

It is very much in the customer's own interest that he states in the purchasing specification the type of packaging required or the probable period of storage. Failure to do this could result in unsuitable packaging and printed boards that are very difficult to solder at the assembly stage.

It is important that the materials used for packaging printed boards are not themselves a source of contamination.

For guidance a few of the materials that are in general use are listed together with information on the degree of protection provided and relative cost.

**10.2 Materials**

**10.2.1** *Sulphur-Free Tissue Paper* — This material is the least expensive and should be used only where the storage conditions are known to be good and the storage period will be of short duration.

The boards should be individually fully wrapped and placed in suitable quantities in a container such as a cardboard box.

**10.2.2** *Polyethylene Sealed Bags* — 0·1 mm ( one hundred gauge ) polyethylene. This material will give good protection for a long period — in excess of 12 months — under good or moderately adverse storage conditions or for a short period under severe storage conditions.

Polyethylene may have diffusion problems and should not be used where there will be prolonged high humidity. The bags should be sealed, preferably by heat fusion. The cost may be moderately low depending upon the quantity of boards in one bag.

**10.2.3** *Laminated Plastic Sealed Bags* — Laminated plastic materials are more expensive than polyethylene but have the advantages of being much stronger and less affected by diffusion problems. They will give good protection over a long period of storage even under adverse conditions and prolonged high humidity. Typical examples of materials are polyethylene/polyamide and polyester/polyethylene, possibly with a lacquer surface coating. Specialist suppliers should be consulted for specific detailed information on suitable materials.

Bags made from laminated plastics should be sealed by the method recommended by the material supplier.

**10.2.4** *Laminated Plastic/Aluminium Bags* — A single layer of aluminium foil with polyethylene or polyester surface films. These laminates are expensive but give extremely good protection for long periods of storage under the most adverse environmental pollution and humidity.

The bags should be hermetically sealed by the method recommended by the material supplier. They have the disadvantage that the contents cannot be checked without opening. Specialist suppliers should be consulted for specific detailed information.

NOTE — All plastic materials and bags intended to be used as storage devices and to protect solderability shall be free of mould release compounds such as silicone which would be a detriment to solderability. The use of a desiccant will normally prolong the possible storage time.

**10.3 Procedures**

**10.3.1** *Pre-Packaging Conditioning* — The boards shall be dried to remove moisture.

The temperature and the time of drying shall be compatible with the base material and/or finish.

Suitable protective gloves shall be used when handling the boards to minimize contamination during packaging.

**10.3.2** *Packaging* — The cost of the materials referred to in **10.2.2, 10.2.3** and **10.2.4** can be reduced by putting a number of boards into one bag. In this case the boards may be interleaved with a layer of sulphur-free tissue paper or other suitable materials of the same size as the boards to protect them from abrasion damage. To avoid that the same package has to be opened several times, the number of boards in one bag should be agreed upon between purchaser and vendor.

NOTE — As tissue paper is hygroscopic, it should preferably be dried to remove moisture prior to inclusion in the plastic bag.

**10.3.3** *Delivery Inspection* — An advantage of clear plastic bags is that the contents can be given a simple visual examination without opening the package.

Full inspection of the boards on delivery may be difficult or impossible without removal of the packaging. Two possible ways of avoiding removal of the packaging are:

— pre-pack inspection at the vendors, or
— packaging after receipt and inspection.

**10.3.4** *Removal of Packaging* — The packaging should be removed not more than 48 h before assembly and soldering.

# APPENDIX A

( *Clause* 6.1 )

## GRID SYSTEM FOR PRINTED CIRCUITS

**A-0.** The grid system for printed circuits shall be used to ensure compatibility between the printed circuits and parts to be mounted on them at the intersection of the grid.

### A-1. DIMENSIONS

**A-1.1** Where individual spacings are required to be 0·635 mm or over, a grid with nominal spacings in the two directions of 2·54 mm shall be used for positioning connections on a printed board.

**A-1.1.1** Where a grid with smaller spacings is necessary, 0·635 mm, shall be used. This secondary grid shall not be further sub-divided.

**A-1.2** Where individual spacings are required to be less than 0·635 mm, a grid with nominal spacings in the two directions of 0·1 mm shall be used for positioning connections on a printed board.

**A-1.2.1** Where a grid with larger spacings, but smaller than 0·635 mm, is essential, a grid of 0·5 mm is recommended.

**A-1.2.2** If subdivisions are necessary, the spacing of the grid shall be obtained by dividing 0·1 mm by 10 or a power of 10.

# BUREAU OF INDIAN STANDARDS


*Headquarters*:

Manak Bhavan, 9 Bahadur Shah Zafar Marg, NEW DELHI 110002

Telephones: 331 01 31, 331 13 75 Telegrams: Manaksanstha (Common to all Offices)


| *Regional Offices*: | *Telephone* |
|---|---|
| Central : Manak Bhavan, 9 Bahadur Shah Zafar Marg, NEW DELHI 110002 | 331 01 31<br>331 13 75 |
| *Eastern : 1/14 C. I. T. Scheme VII M, V. I. P. Road, Maniktola, CALCUTTA 700054 | 36 24 99 |
| Northern : SCO 445-446, Sector 35-C, CHANDIGARH 160036 | 2 18 43<br>3 16 41 |
| Southern : C. I. T. Campus, MADRAS 600113 | 41 24 42<br>41 25 19<br>41 29 16 |
| †Western : Manakalaya, E9 MIDC, Marol, Andheri (East), BOMBAY 400093 | 6 32 92 95 |
| *Branch Offices*: | |
| 'Pushpak', Nurmohamed Shaikh Marg, Khanpur, AHMADABAD 380001 | 2 63 48<br>2 63 49 |
| ‡Peenya Industrial Area 1st Stage, Bangalore Tumkur Road BANGALORE 560058 | 38 49 55<br>38 49 56 |
| Gangotri Complex, 5th Floor, Bhadbhada Road, T. T. Nagar, BHOPAL 462003 | 6 67 16 |
| Plot No. 82/83, Lewis Road, BHUBANESHWAR 751002 | 5 36 27 |
| 53/5, Ward No. 29, R.G. Barua Road, 5th Byelane, GUWAHATI 781003 | 3 31 77 |
| 5-8-56C L. N. Gupta Marg (Nampally Station Road), HYDERABAD 500001 | 23 10 83 |
| R14 Yudhister Marg, C Scheme, JAIPUR 302005 | 6 34 71<br>6 98 32 |
| 117/418 B Sarvodaya Nagar, KANPUR 208005 | 21 68 76<br>21 82 92 |
| Patliputra Industrial Estate, PATNA 800013 | 6 23 05 |
| T.C. No. 14/1421, University P.O., Palayam TRIVANDRUM 695035 | 6 21 04<br>6 21 17 |
| *Inspection Offices* (With Sale Point): | |
| Pushpanjali, First Floor, 205-A West High Court Road, Shankar Nagar Square, NAGPUR 440010 | 2 51 71 |
| Institution of Engineers (India) Building, 1332 Shivaji Nagar, PUNE 411005 | 5 24 35 |

*Sales Office in Calcutta is at 5 Chowringhee Approach, P. O. Princep Street, Calcutta 700072 27 68 00

†Sales Office in Bombay is at Novelty Chambers, Grant Road, Bombay 400007 89 65 28

‡Sales Office in Bangalore is at Unity Building, Narasimharaja Square, Bangalore 560002 22 36 71


Reprography Unit, BIS, New Delhi, India